A 2 Gb/s Throughput GaAs Digital Time Switch LSI using LSCFL

TOHRU TAKADA, YOSHIHIRO SHIMAZU, KIMIYOSHI YAMASAKI, MINORU TOGASHI, KEIGO HOSHIKAWA, AND MASAO IDDA

Abstract—**A GaAs four-channel digital time switch LSI with a 2.0-Gb/s throughput is developed. This switch consists of 4-bit shift registers, data latches, a counter, a control unit, and I/O buffer gates. The LSI includes 1176 devices (FET's, diodes, and resistors) and its equivalent gate number is 231 gates. Low Power Source Coupled FET Logic (LSCFL) operating in a true/complementary mode is used to ensure high-speed and low-power performance. MESFET's with 0.55-μm gate length are fabricated by the buried p-layer SAINT process, which satisfactorily suppresses short channel effects. Dislocation-free wafers are also used to provide high chip yields of 75 percent. The propagation delay time of the LSCFL basic circuit is 48 ps/gate with 1.4-mW/equivalent gate. The total power dissipation including input and output buffers is 0.64 W. The LSI speed performance is evaluated by measuring toggle frequency of the 1/4 frequency divider. The divider operates typically at 5.1 GHz, maximum 7.5 GHz. The newly developed high-speed digital time switch LSI makes possible time division switching services in TV and high-definition TV transmission systems.**

I. Introduction

RECENTLY, digital data processing in the giga-bit rate range has become increasingly important for construction of the Information Network System (INS). Plans for new services in future networks such as high-speed facsimile and high bit rate data transmission (channel data rate: 384 Kb/s–1.5 Mb/s), video conferencing (768 Kb/s–6.3 Mb/s), conventional TV, and high-definition TV (32 Mb/s–400 Mb/s), are now under consideration. The time division technique is preferable for the switching of these services since it fits in better with the digital transmission system than with the space division technique. Thus, digital time switch LSI's are essential devices for exchanging data on a time multiplexed data highway. LSI's with throughput up to 192 Mb/s [1] have already been obtained from Si LSI technology. Throughput is defined as channel number times channel data rate. Commercial digital time switch throughput is currently at a level of only 64 Mb/s for telephone data exchange.

A four-channel digital time switch LSI with a 2.0-Gb/s throughput (channel data rate: 500 Mb/s) was developed using GaAs MESFET technology. In this circuit, operation data rate is 2.0 Gb/s (clock frequency: 2.0 GHz). The channel data rate is sufficient for application to conventional 32 Mb/s TV data. Furthermore, it can be applied to 100 Mb/s (or more) high-definition TV data transmission systems.

In current GaAs sequential logic technology [2], speed performance obtained during the experiment is the fastest to date (divider toggle frequency: type.5.1 GHz, max.7.5 GHz). Also, power dissipation is the lowest, and the integrated device number of 1176 devices is the largest yet obtained.

Three new aspects of GaAs LSI technology helped to achieve these performances and a 75-percent chip yield. First, a new circuit configuration was applied, named Low Power Source Coupled FET Logic (LSCFL). Second, a buried p-layer SAINT process [3] (BP-SAINT) was used, which fabricated 0.55-μm gate-length FET's. Third, dislocation-free, semi-insulating wafers were processed. These wafers were grown by the FEC method [4].

Section II describes the circuit configuration of the digital time switch and LSCFL basic circuit performances. Section III summarizes the fabrication process. In section IV, the measurement system and measurement results of the fabricated digital time switch LSI are described.

II. Circuit Configuration

A. Time Switch Configuration

The digital time switch functions as a data exchange from input- into output-exchanged serial channel data. The switch has address inputs to control output channel order. A buffer memory to store a data frame is necessary in the switch. Generally, random access memory (RAM) is used as the buffer memory and the switching function is realized by changing the order of WRITE data to that of READ data. In this method, the switching speed is limited by the access time of the RAM. It is difficult to achieve a giga-bit rate time switch using the RAM method. A time switch structure using shift registers as a buffer memory was designed, which is shown in Fig. 1. The switching principle is as follows. An input shift register (ISR) reads one signal data frame on a bit-by-bit basis. Using a frame pulse, an input data latch (IDL) takes in the frame data at one time and stores them until the next frame pulse comes. On the other hand, each word of an address control shift registers (ACS) in a control unit (CRU) stores the address of input data in binary form. These address data shift synchronously with the output channel of an output shift register (OSR). Each decoder circuit sends out a latch signal to the output

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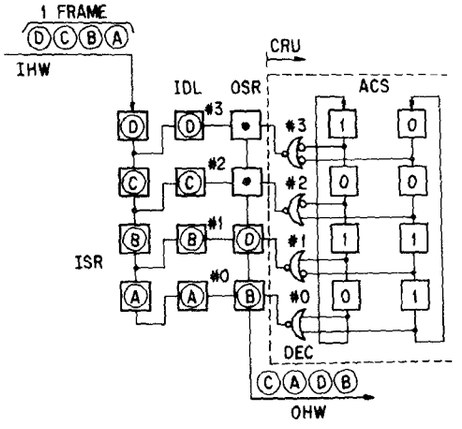

Fig. 1. Digital time switch structure using shift registers. IHW, OHW, ISR, OSR, IDL, ACS, DEC, and CRU mean input highway, output highway, input shift register, output shift register, input data latch, address control shift registers, decoder and control unit, respectively.

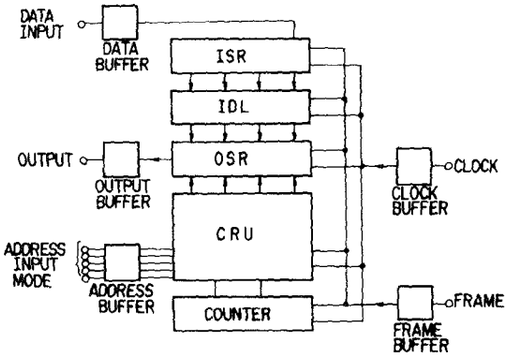

Fig. 2. Block diagram of digital time switch.

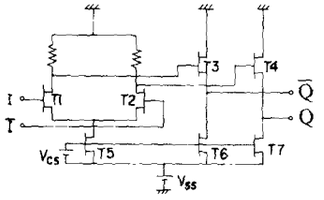

Fig. 3. LSCFL basic configuration (inverter).

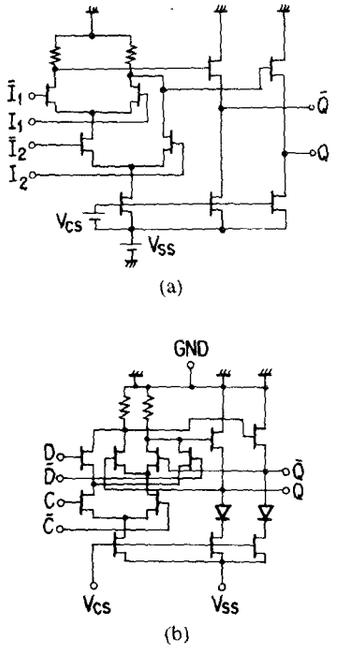

Fig. 4. (a) Series gate configuration (two inputs NOR). (b) Series gate configuration ($R-S$ flip-flop).

channel, but only when the same address as that of the decoder comes from the ACS. Then, the OSR accepts the input data using the latch signal and reads out the latched data. Here, the address data is written into the uppermost cell of the ACS with a determined timing which is controlled by a counter and comparator.

A LSI block diagram is shown in Fig. 2. Each circuit block is constructed mainly with R-S F/F's, D-F/F's, T-F/F's, and 2-input OR/NOR gates. The total equivalent gate number is 231 gates. The maximum operation data rate is determined from the expression $1/(6\tau_{pd})$. Here, τ_{pd} is the mean propagation delay time of the internal series gates. Thus, the LSI operates at about 1/3 the toggle frequency of a frequency divider circuit operating at $1/(2\tau_{pd})$. Internal gate dissipation power is 1.4 mw per equivalent gate using a 20-μm FET gate width. Output, frame, and clock buffers dissipate 20, 30, and 70 mW of power, respectively. Input buffers (data, clock, frame, and address) convert the ECL logic level into the LSCFL level, defined as 0 V ~ −0.45 V. The output buffer with a 100-Ω output impedance provides a 0.45-V LSCFL level.

B. LSCFL

The LSCFL circuit configuration was applied to the LSI. The basic configuration of the LSCFL is shown in Fig. 3. The LSCFL has true (I, Q) and complementary $(\bar{I}, \bar{Q})$ signal terminals at inputs and outputs. The LSCFL does not have a reference dc terminal like a conventional SCFL [5] or ECL. Instead, series gating is used as shown in Fig. 4(a) and (b). The true and complementary (T/C) operation in LSCFL circuits enables the logic swing (V_{LS}) to be half of the reference used in the SCFL circuits, where $\bar{I}$ and $\bar{C}$ are used as reference dc voltage terminals. This is because the transfer gain using T/C signals is twice as large as the SCFL operation using a dc reference. The half V_{LS} represents half load resistance R_L, which implies higher speeds. It also requires a smaller voltage source magnitude V_{SS} implying lower power dissipation. FET's in LSCFL are enhancement-mode FET's (EFET). EFET's implementation also requires a smaller V_{ss} magnitude in addition to the T/C operation. Thus, LSCFL realizes low-power performance.

V_{LS} and V_{SS} were determined to be 0.45 V and −2.5 V, respectively, using a +0.2-V FET threshold voltage V_{th}. The propagation delay time (t_{pd}) histograms of the LSCFL circuit measured for a 2-in wafer are shown in Fig. 5(a); Fig. 5(b) shows the power dissipation. These data were obtained from ring oscillators which consist of the inverters shown in Fig. 3. $Wg1$ is the gate width of $T1$, $T2$, and $T5$.

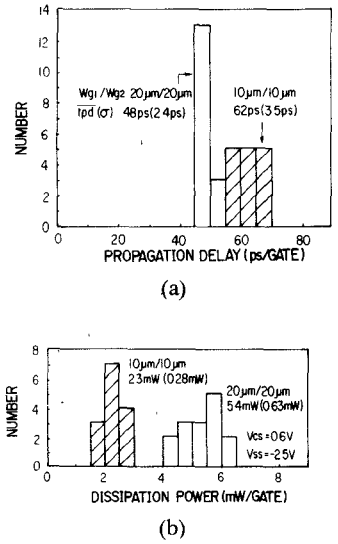

Fig. 5. (a) Histogram of propagation delay. (b) Histogram of power dissipation.

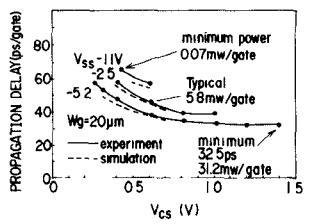

Fig. 6. V_{ss} and V_{cs} dependence of propagation delay.

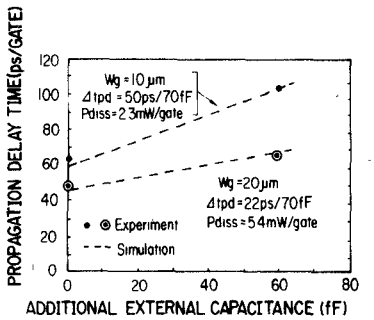

Fig. 7. Evaluation of capacitance drive capability.

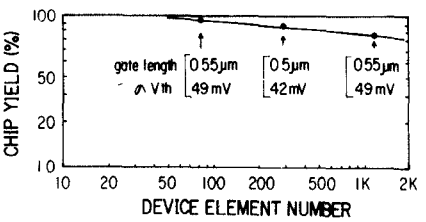

Fig. 8. Chip yield of IC's by LSCFL.

$Wg2$ is gate width of $T3$, $T4$, $T6$, and $T7$. Other device parameters of the FET's are given in Section III. Load resistances in the 10μm/10μm circuit are twice as large as those of the 20 μm/20 μm circuit. The ratios of $Wg1$ and $Wg2$ were optimized to be 1/1 by computer simulation. It can be seen that the larger gate-width FET's provide higher speed. This phenomenon indicates the existence of parasitic capacitances which are not proportional to gate width [6], [7]. It is thought that these capacitances can be attributed mainly to static edge capacitances of gate, source, and drain electrodes. In Fig. 5(a), it should also be noted that the standard deviation of t_{pd} is very small (2.4 ps), in addition to the small t_{pd} of 48 ps. The t_{pd} for the E/D DCFL circuit, which was fabricated on the same wafer, varied from 80 ps to 350 ps. The small deviation of t_{pd} is one of the desirable features of the LSCFL. This feature is especially effective in sequential logics in which a maximum operation data rate is determined by t_{pd} of the lowest speed gate.

An average power dissipation of 5.4 mW is effectively reduced to 1.4 mW/(equivalent gate) when a series gate configuration such as shown in Fig. 4(b) is used. This is because from NOR gates are necessary if the circuit is to be constructed with 2-input NOR gates. Almost all of the gates in the digital time switch LSI were reduced in power by using this series-gating configuration. The value of 1.4 mW/gate is much smaller than other GaAs high-speed logics, such as BFL (10 mW/gate), and is a bit larger than DCFL.

Typical V_{cs} and V_{ss} values are 0.6 V and -2.5 V; however, LSCFL operates over a wide range of voltage-source magnitudes. Fig. 6 shows a V_{cs} dependence of t_{pd} as a parameter of V_{ss}. The solid and broken lines indicate experimental and simulated results, respectively. A minimum t_{pd} of 32.5 ps was obtained with 31.2 mW/gate for 1.4-V V_{CS} and -5.2-V V_{SS}. Minimum power dissipation was 0.07 mW/gate for 0.4-V V_{cs} and -1.1-V V_{ss}. In this case, t_{pd} was 65 ps. These results were obtained for a gate width of 20 μm. FET's with 2.0-μm gate width have already been fabricated by the latest GaAs process technology [8]. If 2.0-μm gate-width FET's are used, power dissipation is reduced to 7 μW/gate. This power implies VLSI possibility.

The interconnection line drive capability was also evaluated with ring oscillators which load capacitances intentionally at Q and $\bar{Q}$ terminals in Fig. 3. The propagation delay time as a function of additional capacitance is shown in Fig. 7. The line capacitance on a GaAs semi-insulated substate is approximately 70 pF/mm. Assuming this value, an incremental delay for a 1-mm line addition is calculated to be 22 ps/mm for 20-μm gate-width FET's. This value is the lowest to date in any device for LSI, including Si bipolar transistors [9]. The large drive capability of LSCFL results from the existence of source followers.

The logic swing in LSCFL is small compared with other GaAs MESFET logics, as mentioned above. However, the T/C operation protects correct logic operation from fairly large V_{th} deviations and scatterings. Simulation results show that LSCFL permits a deviation range of $+0.2/-0.3$ V for 0.2-V centered V_{th}, assuming 0-V standard deviation of scattering. The T/C operation corresponds the operation when reference voltages of individual internal gates in a conventional SCFL are adjusted individually in order to provide correct operation. Fig. 8 shows the experimental

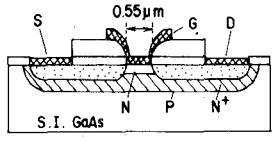

Fig. 9. Structure of BP-SAINT.

TABLE I
BP-SAINT FABRICATION PROCESS

Substrate	Dislocation-free FEC
	Photo-lithography 10: Stepper
Channel Layer	Si^+, 67 keV, $2.2\times10^{12}cm^{-2}$ dose
n^+ Layer	Si^+, 200 keV, $4.0\times10^{13}cm^{-2}$ dose
p^+ layer	Be^+, 90 keV, 6.0×10^{11} cm^{-2} dose
Load Resistor	Si^+, 67 keV, 9.0×10^{12} cm^{-2} dose
Interconnection	1.5-μm line/space
Gate length	0.55 μm
V_{th}	0.18 V
αV_{th}	49 mV
g_m	160 mS/mm
Load Resistor, R_L	880 ohm°
$\alpha R_L/R_L$	1.8%

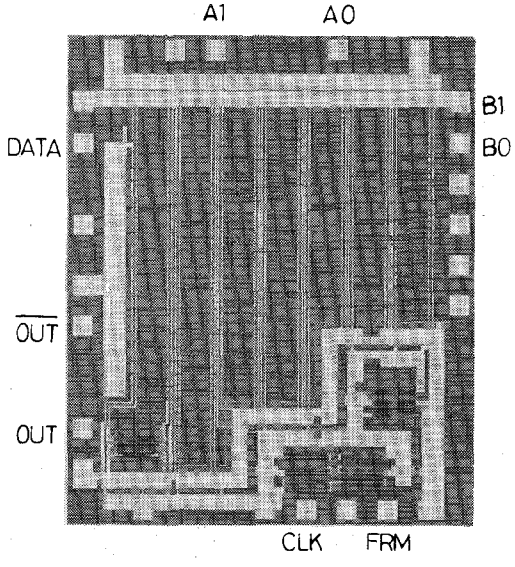

Fig. 10. Microphotograph of digital time switch LSI.

chip yield of LSCFL IC's fabricated in our laboratory as a function of the device element number. A high chip yield possibility is also an LSCFL advantage.

III. FABRICATION PROCESS

Gate-length shortening is the most effective method for obtaining high-performance FET's. However, FET's with submicron gate lengths cause undesirable short channel effects, such as V_{th} reduction, large sub-threshold current, and V_{th} scattering increases. The buried p-layer SAINT process [3] was applied to decrease the short channel effects. As a result, 0.55-μm gate-length FET's were successfully fabricated using photolithography with a 1/10 reduction stepper. In this process, a p-type layer is formed under the active layer to suppress substrate current by Be^+ implantation. The FET structure is shown in Fig. 9. Dislocations in LEC-grown GaAs crystals induce V_{th} scattering

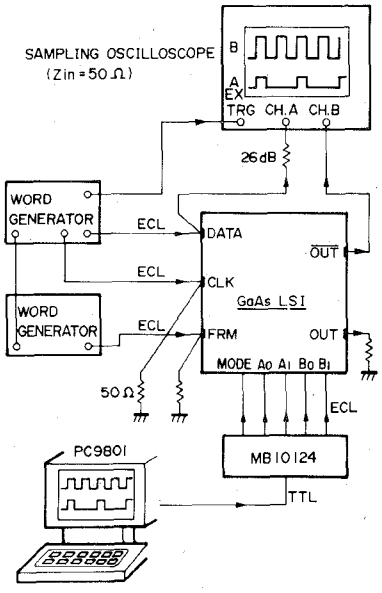

Fig. 11. 2.0-Gb/s measurement system.

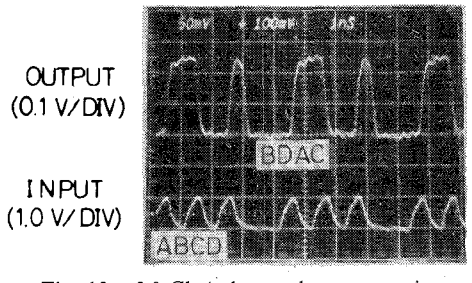

Fig. 12. 2.0-Gb/s data exchange operation.

[10]. Thus, dislocation-free wafers were used, which were obtained from the FEC method combined with indium doping [4]. A small measured V_{th} standard deviation of 49 mV in spite of submicron gate FET's is due to these wafers, as well as to the buried p-layer FET process.

A brief description of the fabrication process and results are summarized in Table I. A microphotograph of the fabricated digital time switch LSI is shown in Fig. 10. Chip size is 2.0×2.4 mm.

IV. MEASUREMENT RESULTS

The measurement system was arranged with two 2.0-Gb/s word generators, a sampling oscilloscope, on-wafer probe card equipment, TTL–ECL transition IC's and a personal computer. This arrangement is shown in Fig. 11. A PC9801 personal computer controlled the address input test pulse patterns. The two types of input data and eight types of address data were used, as test patterns. Expected output patterns corresponding to input patterns, displayed on the computer CRT, were compared with measured output waveforms on the oscilloscope. The fabricated LSI operated correctly for all test patterns up to and including the 2.0-Gb/s input data rate. Dissipation power was 0.64 W. A 2.0-Gb/s data exchange operation is shown in Fig. 12. It can be seen that the input channel order *ABCD* is changed into the output channel order *BDAC*. The LSI

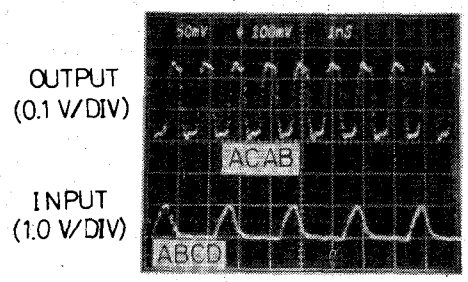

Fig. 13. Plural writing exchange operation. Input channel data A is written on two output channels.

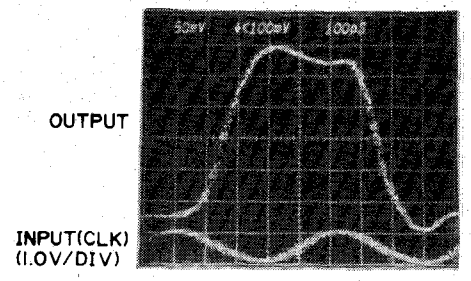

Fig. 14. Output wave rise/fall time measurement result.

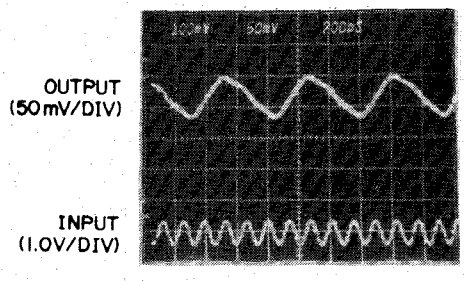

Fig. 15. 7.5-GHz operation of 1/4 divider.

also has a switching function for broadcasting services, which puts the same input data on plural output channels. This is shown in Fig. 13. The range for correct operation V_{SS} is from -1.7 to -3.0 V. Output wave rise and fall times (20–80 percent) are 90 and 80 ps, respectively, as shown in Fig. 14. The fabrication yield reached 63 percent for designed bias and 75 percent for adjusted bias. (V_{SS} is -2.5 V for both conditions.)

One-quarter frequency dividers were fabricated to evaluate the internal gate operation speed. These dividers had the same circuit configuration and device parameters, and were fabricated on the same wafer as the digital time switch. This divider operated up to 5.1 GHz with 45 mW of dissipation power ($V_{ss} = -2.5$ V). This result is reasonable, though the speed is not three times the maximum operation speed (2.0 Gb/s) of the digital time switch. This is because the digital time switch includes OR/NOR gates of $F0 = 1$ having smaller propagation delay times than for the divider ($F0 = 3$).

The divider toggle frequency increased to 7.5 GHz by increasing V_{ss} and V_{cs} (dissipation power was 277 mW), as shown in Fig. 15. This value is currently the highest of any frequency divider fabricated using GaAs MESFET's and HEMT's at room temperature.

The switching system for color TV data (64-Mb/s channel data rate) was actually constructed and demonstrated with the developed GaAs digital time switch LSI. The system consists of the GaAS LSI and commercial Si bipolar IC's such as A/D converters, D/A converters, multiplexers, demultiplexers, video amplifiers, and other SSI gates. The system operated successfully up to 300 Mb/s. The maximum data rate is limited by the maximum operation rate of Si bipolar IC's in this system.

V. Conclusion

A 2.0-Gb/s throughput four-channel GaAs digital time switch LSI was developed using a new circuit configuration (Low Power Source Coupled FET Logic), a new fabrication process (0.55-μm gate buried p-layer SAINT), and dislocation-free wafers. In addition to high-speed (48 ps/gate, 22 ps/mm) and low-power (1.4 mW/equivalent gate) performances, a high fabrication yield of 75 percent was achieved. The LSI speed was also evaluated by toggle frequencies of 1/4 frequency dividers, in addition to ring oscillators. The divider operated at a maximum 7.5 GHz. Using the GaAs digital time switch LSI, the color TV data switching system was actually constructed together with Si bipolar IC's . The LSI will have a favorable impact on realizing giga-bit rate digital network systems in the near future.

Acknowledgment

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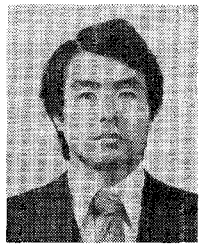

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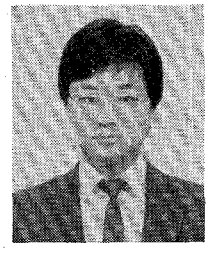

Yoshihiro Shimazu was born in Tokyo, Japan, on February 26, 1958. He graduated from Tokyo Institute of Technology with a B.E. degree in 1980 and a M.E. in 1982 in applied physics and energy science, respectively.

In 1982, he joined N.T.T. as a member of the Musashino Electrical Communication Laboratory, where he has been engaged in research on high speed switching systems. Recently, he has been engaged in the development of high-speed transmission systems at Yokosuka Electrical Communication laboratory.

Mr. Shimazu is a member of the Institute of Electronics and Communication Engineer of Japan.

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Kimiyoshi Yamasaki was born in Ehime Prefecture, Japan, on May 4, 1952. He received the B.E., M.E., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1975, 1977, and 1980, respectively.

In 1980, he joined the Musashino Electrical Communication Laboratory, NTT, Tokyo, Japan. He is now engaged in the research and development of GaAS devices and process technology for high-speed IC's as a Staff Engineer at the NTT Atsugi Electrical Communication Laboratories, Atsugi-shi, Kanagawa Prefecture, Japan.

Dr. Yamasaki is a member of the Japan Society of Applied Physics and the Institute of Electronics and Communication Engineers of Japan.

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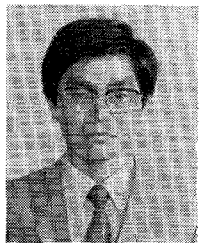

Minoru Togashi was born in Miyagi, Japan, on October 2, 1955. He received the B.S. and M.S. degrees in electronics engineering from Tohoku University, Sendai, Japan, in 1979 and 1981, respectively.

He joined Musashino Electrical Communication Laboratories, NTT, Tokyo, in 1981. Since then he has been engaged in research and development on GaAs IC design. He is currently an Engineer at the NTT Atugi Laboratories.

Mr. Togashi is a member of the Institute of the Electronics and Communication Engineers of Japan.

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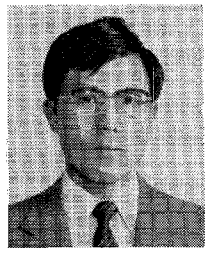

Keigo Hoshikawa received the B.S. and M.S. degrees from Shinshu University, Japan, in 1967 and 1969, respectively.

He joined the NTT Atugi Electrical Communication Laboratories in 1969 and worked on growth and characterization of silicon crystals for LSI. Since 1982, he has been engaged in research and development on semi-insulating LEC GaAs crystal for GaAs LSI's.

Mr. Hoshikawa is a member of the Electrochemical Society, the Japan Society of Applied Physics, Crystallographic Society of Japan, and the Institute of Electronics Communication Engineers of Japan.

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Masao Idda was born in Yokohama, Japan, on September 25, 1944. He received the B.S. degree in electronic engineering from Nagoya University, Nagoya, Japan, in 1967.

In 1967, he joined the NTT Electrical Communication Laboratory, Tokyo, Japan, where he worked on GaAs Schottky diodes for millimeter-wave systems and their reliability, and the development of GaAs MESFET's and InP MESFET's. He is now engaged in the design of GaAs LSI's as a Staff Engineer at the Atsugi Electrical Communication Laboratories, NTT.

Mr. Idda is a member of the Institute of Electronics and Communication Engineers of Japan.